

	U	1	Document ID	Title	Current OR	Pages	Issue Date
1	<input type="checkbox"/>	<input type="checkbox"/>	US 5838038 A	Dynamic random access memory device with the combined open/folded bit-line pair arrangement	257/301	49	19981117
2	<input type="checkbox"/>	<input type="checkbox"/>	US 5523259 A	Method of forming metal layers formed as a composite of sub-layers using Ti texture control layer	438/643	9	19960604
3	<input type="checkbox"/>	<input type="checkbox"/>	KR 9209749 B	High integration memory device mfr. for NMOS cell - includes patterning field area on silicon substrate, growing epitaxial layer, removing field oxide film and forming diffusion region		NA	19921022

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	47198	(epitaxial) near15 (substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM-TDB	2004/02/20 10:33	
2	BRS	L2	542	(epitaxial) near15 (substrate) near15 (active near region)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM-TDB	2004/02/20 10:34	
3	BRS	L3	13	(epitaxial) near15 (substrate) near15 (active near region) near25 (opposite)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM-TDB	2004/02/20 10:34	